A HETEROGENOUS SIP SOLUTION FOR RF APPLICATIONS

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***Abstract*— An interposer with embedded IC's has been fabricated in support of BAE Systems and Georgia Tech Research Institute using a Heterogeneous System In a Package (HSIP) technology for the purpose of creating a new and highly integrated RF MCM solution. The HSIP technology is based on well-established FOWLP (Fan-Out Wafer Level Packaging) technologies consisting of a double sided interconnect wafer fabrication process with the target IC's embedded in the HSIP interposer core. Signals are carried from front to back of the device using through-mold-via. The resulting interposer is stackable and can receive a BAE Systems MMIC die by flip chip assembly, and be subsequently stacked to a RF printed circuit main board.**

In this paper, we discuss some of the key fabrication details of the HSIP device construction itself. We present an overview of selected design for manufacturability considerations, as well as the geometrical and mechanical properties of the resulting HSIP interposer devices.

Keywords—phased array, MCM, multi-chip module, HSIP, interposer, embedded IC, FO-WLP.

I. INTRODUCTION

A team led by Georgia Tech Research Institute (GTRI) with design and fabrication support from BAE System (BAE), i3 Technologies, and Aurora Semiconductor LLC ("Aurora") is developing the 2-12 GHz wideband reconfigurable array elements suitable for future phased array applications [1]. The program, sponsored by the U.S. Defense Advanced Research Projects Agency (DARPA) in Arlington, Va., is called Arrays at Commercial Timescales (ACT) program. It allows for a 2D tile-able array of elements, for a truly scalable and reconfigurable phased array element achieved through vertical integration of devices in a reliable heterogeneous solution.

In this program, BAE Systems has designed and fabricated an arbitrary current control circuit using their GaAs MMIC (Monolithic Microwave Integrated Circuit) technology. A Heterogeneous System In a Package (HSIP) module is also designed, in which both active and passive components are embedded into a molded wafer substrate to act as an interposer between the aforementioned MMIC and an RF printed circuit board. In this fabrication approach, various established FOWLP (Fan-Out Wafer Level Packaging) techniques are utilized resulting in a double-sided interconnected device with 4 interconnect metal layers per side. This double sided interconnect technology is made possible by using Through Mold Via (TMV) that provide the front to back signal handling through the core of the interposer. The GaAs MMIC device is then mounted directly onto the top side of this HSIP module by i3 Electronics using established GaAs flip chip techniques. Finally, the completed, stacked sub-assembly of MMIC over HSIP module is mounted to a main RF board by GTRI for final testing.

II. HSIP FABRICATION

The HSIP technology has a long history of integrating many IC's and passives into multi-chip modules for maximum silicon packing. In the case of this project, the majority of the device core volume would instead be mold compound and not the usual densely packed silicon components. The HSIP technology design rule guidance calls for a percentage die volume minimum of 40% whereas this design would be fabricated at 23%. The fabrication implication was that there were more substantial concerns regarding die shift as a function of molding the FOWLP wafer, due to the liquefied flow and cure dynamics of the mold compound, than with previous products. The proprietary HSIP baseline process takes this into account through use of module-level

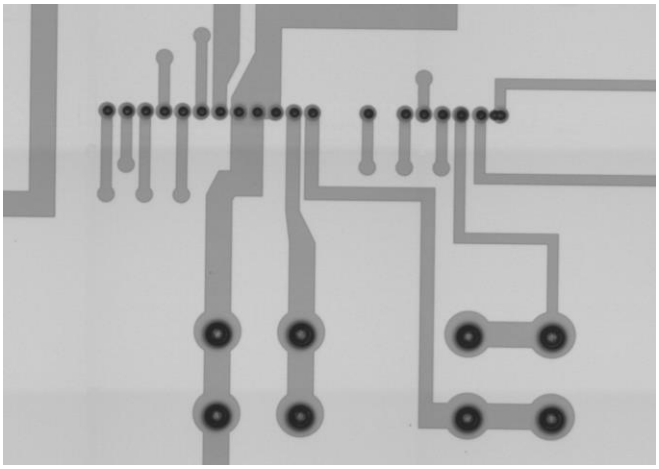

Figure 1. Automated Inspection Scan of interconnect layer routing over the IC components on the HSIP embedded interposer fabricated for the DARPA ACT program. The image shows good alignment of the first HSIP layers to the embedded IC component.

algorithmic solutions for placement of the first layer of via and metal patterns, solved to the constellation of IC and passive components on a module by module basis, such that the individual via land completely on the bond pads of the components, and such that the first metal layer of the HSIP can fully enclose those via, as shown in Figure 1.

Even so, initial testing indicated die shift average magnitudes of close to 18 microns, with a standard deviation of 11 microns. This level of performance while possibly acceptable for prototyping would otherwise limit the starting molded wafer yield to approximately 90% given the expected limitations of the algorithms explained earlier. Through several targeted Design Of Experiments (DOE) focused on the manner in which the die are made to adhere to the wafer molding temporary carrier, and how temperature was to be applied during molding, these two values were able to be lowered to 9.2 and 5.3 microns, respectively, with a resulting starting molded wafer yield of 100%.

To assist in achieving flatness across the final HSIP module, the embedded IC were placed in a symmetrical arrangement. The particular IC component being embedded has 67 pads requiring I/O to be routed through the HSIP either to the 151 top-side MMIC pads or to the 36 bottom-side (board side) pads. With the exception of having redundancy, only 36 of the signals must be passed through the core of the HSIP interposer using the TMV, but in order to reduce metal area that could interfere with the RF performance, the TMV were subdivided to grouped areas of the module in such a way that a total of 8 TMV banks where utilized in the design. This could easily be simplified on future design-ins, since each bank contained 40 TMV but required fewer than 20 pass through per bank location.

The metal fill percentage per layer as shown in Table I are a resulting function of routing the interconnections for the aforementioned I/O quantities to the front and back of the HSIP device up to the bond pads for the MMIC or through the TMV down to the RF main board. The values are quite low when compared to other typical digital HSIP designs in production; digital HSIP designs frequently having high fill percentages for features such as ground and power planes.

HSIP Device Layer	***Percent Fill***
Front Metal 1	5.8
Front Metal 2	4.4
Front Metal 3	0.6
Front Metal 4	7.4
Front Pad Metal	2.2
Back Metal 1	3.1
Back Metal 2	3.0
Back Metal 3	2.2
Back Metal 4	4.8
Back Pad Metal	3.1

TABLE I. METAL FILL PERCENTAGE PER LAYER

The front to back distribution of the metal area was fairly well-balanced by design, to achieve the best possible neutrality of the device bow characteristics over temperature; the front metal area totaled 20.3% while the back metal area totaled 16.3%. This 4% difference is quite favorable versus many existing HSIP designs for digital solutions and contributed to excellent flatness of the final module prior to MMIC flip chip assembly.

The expected final flatness of the fabricated modules were targeted at better than 2.5 micron per millimeter across the entire interposer for a total bow not greater than 36 microns over the 14.6 x 14.6 millimeter area of the module. Final fabrication measurements indicated that module flatness was excellent at an average total bow of 14.5 microns with a standard deviation of 11.2 microns or essentially 1 micron per millimeter versus the targeted flatness of 2.5 microns per millimeter.

The completed HSIP modules are relatively thin packaged devices. Their total thickness as fabricated averaged 346.4 microns with a standard deviation of 7.0 microns, with the majority of the variation coming from the temporary carrier processes that are present during wafer thinning. Based on previous finite element analysis it is expected that the Coefficient of Thermal Expansion of the HSIP module would be about 10 ppm per degree Celsius but had not yet been confirmed when this paper was published.

III. HSIP FABRICATION RESULTS

The HSIP wafer Phase 1 build consisted of 4 wafers with 21 candidate modules per wafer. From these wafers a total of 63 modules conformed to all product specifications and quality requirements for a first prototype build fabrication yield of 75%. The modules were then further assembled via a flip chip technique used to mount the MMIC die to the HSIP module using available assembly processes at i3 Technologies. The HSIP itself is much more durable in nature at this assembly point than a typical GaAs MMIC die, such that the only modification to typical GaAs assembly technique is the relative alignment of the MMIC to the HSIP, rather than the MMIC down to a board connection. There was no yield loss from this assembly activity once a process was developed and executed.

At the time of this publication, an assembled array using 16 total MMIC-HSIP stacked modules from the conforming units delivered were being tested at GTRI. Preliminary results for band tuning, scan loss recovery, polarization selectivity, and array gain are reported as favorable.

IV. CONCLUSION

The HSIP technology can produce robust electronic components that meet next-generation packaging requirements for tightly packed integrations in order to achieve the lowest power, weight, and size while enabling new and exciting system concepts for designers.

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VI. References

[1] B. McMahon, R. Lapierre, R. Westafer, T. Lee, N. Saldanha, "Arbitrary current control in an array environment by tight integration of the ACT array MMIC and CMOS controllers", GOMAC proceedings, March 2018, Miami FL

[2] T. Lee, et al., "Demonstration of a Wideband Array using Reconfigurable Monolithic Antenna Elements" GOMAC 2017, March 20-25 2017, Reno, NV

[3] 3D IC and 2.5D IC Packaging Market by Application (Logic, Imaging & Optoelectronics, Memory, MEMS/Sensors, LED, Power), Packaging Technology (3D Wafer-Level Chip-Scale Packaging, 3D TSV, 2.5D), End-User Industry, and Region - Global Forecast to 2022, Markets and Markets Research Report, SE 4844, Jan 2017

[4] Tummala, R. & Swaminathan, M. (2008) System on Package: Miniaturization of the Entire System, 3-81.